Profile of Dr. Kaleem Fatima

Dr. Kaleem Fatima is a Professor in the Department Electronics and Communication Engineering , Muffakham Jah College of Engineering and Technology, Hyderabad since 2010. She received her B.E degree in ECE from PDA College of Engineering, in 1988 and M.Tech in Digital Electronics and Communication Engineering from Mysore University in Karnataka in the year 1991. She was awarded Ph.D Degree in ECE from Osmania University, Hyderabad in 2009. She has 30 years of teaching and research experience. She served the department of ECE, MJCET as HOD for 10 years and was member BOS and DRC at Osmania University. Her research interests are in Digital and VLSI Design, algorithms for CAD, Mobile Ad hoc networks and IOT Security. She has published 32 Journal and Conference papers in reputed international journals and Conferences. She has one patent "A Pneumatic Quadruped Robot and a Method of Preventing Accidents Thereof". She is currently supervising 10 Ph.D Scholars. Three scholars are awarded Ph.D degree under her.

Dr. Kaleem Fatima is a senior member of IEEE and Fellow of IETE. She is an active member of IEEE at her college and also at the Hyderabad Section. She received "IEEE Region 10 Outstanding Branch Counselor Award" for the year 2011-2012. She has serving the CAS/EDS Joint Chapter of IEEE Hyderabad Section from 2012 till date in various capacities, like Secretary, Vice-Chair and Chair. She was the organizing chair and publication chair in three "PRIME ASIA IEEE international conferences" conducted by IEEE Hyderabad Section CAS/EDS Chapter.

List of publications- Dr.Kaleem Fatima

I. International Journal

1. Shefali, M., Fatima, K., and Uma Sathyakam, P., "Performance Analysis of CNT Bundle Interconnects in Various Low-k Dielectric Media", Journal of Solid State Science and Technology, vol. 11, no. 6, 2022.
2. Kaleem Fatima and Rameshwar Rao, "FPGA Solution for Multi-layer Maze Routing" IETECH International Engineering and Technology Journal of Communication Techniques, Vol: 2, No: 2, pp 78-83, 2008. (ISSN 0973 8053)
3. Kaleem Fatima and Rameshwar Rao, "A Hardware Router for Multi-Terminal Nets" IETECH International Engineering and Technology Journal of Information Systems. (ISSN 0973 8096)
4. Fauzia, S., Fatima, K," QoS based Routing for Free Space Optical Mobile Ad Hoc Networks.,"2019 International Journal of Vehicle Information and Communication Systems (IJVICS).
5. Fauzia, S., Fatima, K," Routing in Optical Mesh Networks - A QoS Perspective.," 2018 International Journal of Ad hoc, Sensor & Ubiquitous Computing (IJASUC).

6. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Efficient Realization of Vinculum Vedic BCD Multipliers for High Speed Applications" in Journal of Circuits and Systems,2018,vol 9, with ISSN 2153-1293 , DOI:10.4236/cs.2018.96009 June 2018.
7. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Hybrid Signed Digit Parallel and Multi Operand BCD Adders" International Journal of Pure and Applied Mathematics Volume 20, No.6 1337-1391 with ISSN number1314-1395, 2018.
8. Fauzia S., Fatima K. (2018) Performance Evaluation of AODV Routing Protocol for Free Space Optical Mobile Ad-Hoc Networks. In: Thampi S., Mitra S., Mukhopadhyay J., Li KC., James A., Berretti S. (eds) Intelligent Systems Technologies and Applications. ISTA 2017. Advances in Intelligent Systems and Computing, vol 683. Springer, Cham.
9. Nazeerunnisa and Dr.Kaleem Fatima,"ANFIS Based Performance Analysis In Uplink OFDMA Rician Fading Channel", International system of VLSI system design and communication system. ISSN 2322-0929 Vol.03, Issue.07, September-2015.
10. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Area_Delay_Power Efficient Booth Encoded Reversible Multiplier using Compressors" Journal of Innovation in Electronics and Communication Engineering(An International Journal) Jul-Dec 2015 Volume5, Issue2 ISSN: 2249-9946.
11. G.Sree Lakshmi, Dinesh Alapati Dr.Kaleem Fatima, Dr.B.K.Madhavi "High Performance BCD Adder-Subtractor Using Reversible Logic" International Journal of Engineering Inventions Nov-Dec 2012 ISSN: 2278-7461.

II. National Journal

III. International conference

1. L. Prathibha and K. Fatima, "Exploring Security and Authentication Issues in Internet of Things," *2018 Second International Conference on Intelligent Computing and Control Systems (ICICCS)*, Madurai, India, 2018, pp. 673-678.
2. Fauzia, S., Fatima, K,"A New Approach to Directional Routing in MANETs", 2019 IEEE International Conference on Innovative Technologies in Engineering IEEE,ICITE , OU, 2018 978-1-5386-5080- 6/18 (To be published)
3. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Designing of Digital circuits using Vedic mathematics for Engineering Applications" at the 3rd International Vedic Mathematics Conference at RV College of Engineering Bengaluru, 23-25 August 2018.

4. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Hybrid Signed Digit Parallel And Multi Operand BCD Adders" International Conference ICIDEST 17th& 18th April 2018, KCG college of Engineering and Technology, Chennnai.
5. G.Sree Lakshmi, Mohammad Salman, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Efficient Vedic Signed Digit Decimal Adder" Fourth International Conference on Devices, Circuits and Systems (ICDCS'18)ISBN: 978-1-5386-3476-9/18/$31.00 ©2018 IEEE 16th & 17th Mar 2018, Electronics and Communication Engineering Karunya Institute of Technology and Sciences
6. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "A Novel Approach to The Learning Of Vinculum Numbers In Two's Compliment Method For BCD Arithmetic Operations"Proceedings of the Second International Conference on Computing Methodologies and Communication (ICCMC 2018) IEEE Conference Record # 42656; IEEE Xplore ISBN:978-1-5386-3452-3978-1-5386-3452-3/18/$31.00 ©2018 IEEE 475
7. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi" Implementation of High Speed Vedic BCD Multiplier using Vinculum Method" TENCON IEEE conference 22nd to 25th Nov 2016. 978-1-5090-2597-8/16/$31.00 c 2016 IEEE
8. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Compressor Based 8x8 Bit Vedic Multiplier using Reversible Logic" in the 3rd International Conference on Devices, Circuits and Systems (ICDCS'16) held from 3rd to 5th March 2016 at Karunya University, Coimbatore, India.978-1-5090-2309-7/16/$31.00©2016 IEEE
9. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Implementation of High Speed Vedic BCD Multiplier using Vinculum Method" TENCON IEEE conference 22nd to 25th Nov 2016. 978-1-5090-2597-8/16/$31.00 c 2016 IEEE Publisher: IEEE Digital Xplorer
10. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Compressor based 8x8 Bit Vedic Multiplier using Reversible Logic" in the 3rd International Conference on Devices, Circuits and Systems (ICDCS'16) held from 3rd to 5th March 2016 at Karunya University, Coimbatore, India. 978-1-5090-2309-7/16/$31.00©2016 IEEE. Publisher: IEEE Digital Xplorer.
11. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Area_Delay_Power Efficient Booth Encoded Reversible Multiplier using Compressors" 4th International Conference on Innovations in Electronics and Communication Engineering (ICIECE-2015),August 21st -22nd 2015, Hyderabad, India. ISSN 2249-9946 Vol 5 issue 2G.
12. S. Fauzia and K. Fatima, "Routing in FSO MANETs & 2014; QoS and directionality," *2014 Eleventh International Conference on Wireless and Optical Communications Networks (WOCN)*, Vijayawada, 2014, pp. 1-5. doi: 10.1109/WOCN.2014.6923062
13. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "A High Speed Low Power Multiplier-Accumulator Architecture using Higher Radix Modified Booth Algorithm" at 2nd World Conference on Applied Sciences, Engineering & Technology (WCSET 2013)

14. G.Sree Lakshmi, Kaleem Fatima, Dr.B.K.Madhavi, "A Review of Low Power and High Performance Multipliers and their Hardware Implementations" in Proc of International Conference on Advancements in Engineering and Management, ICAEM 2012, RITs College of Engg. 28th – 29th Feb 2012
15. Md. Sabir Hussain, Md. Zakir Hussain, Dr. Kaleem Fatima, "High Speed FSM-Based Programmable Memory Built-In Self Test (MBIST) Controller", Accepted in International Conference On Electronics and Communication Engineering (ICECE 2012), to be held on April 28th -29th, 2012., Vizag, India.
16. Prof. Mrs. Kaleem Fatima, Shyam Sundar Mikkili, and Sriram Sankar "The Design and Implementation of a Multiplexed Multi-layer Maze Router " International Conference On Electronics and Communication Engineering (ICECE 2012), April 28th -29th, 2012., Vizag, India.
17. Hajira fathima , Jahangeer Md, Dr. Kaleem Fatima, "Design of Low Power Shannon Based Adder Cell using Multiplexing Control Input Technique", accepted in International Conference On Electronics and Communication Engineering (ICECE 2012), to be held on April 28th -29th, 2012., Vizag, India.
18. M. A. Raheem and Kaleem Fatima:, "A High Speed Reversible Low Power Error Tolerent Adder" in proceedings of PrimeAsia 2012, held in Dec 7-9, 2012, Bits Pilani, Hyderabad campus.
19. Kaleem Fatima and Rameshwar Rao, "A New Hardware Routing Accelerator for Multi-terminal Nets," *in Proc. of 22nd IEEE Intl. Conf. on VLSI Design*, New Delhi, Jan 5-9 2009, pp393-398.portal.acm.org/citation.cfm?id=1495778; **(ISBN: 978-0-7695-3506-7)**
20. Kaleem Fatima and Rameshwar Rao, "FPGA Implementation of a New Parallel Routing Algorithm*," in Proc. of IEEE R10 Intl. Conf. TENCON 2008,* at Univ. of Hyd, Hyderabad, Nov 19-21 2008.
21. Kaleem Fatima and Rameshwar Rao, "FPGA Implementation of 2D DWT Encoder- A New Approach" in Proc. of ICVLSI '08 International Conference on VLSI and Embedded Systems, Velammal Engineering College, Chennai, India, Feb. 14-16, 2008, pp 169-174.
22. Kaleem Fatima and Rameshwar Rao, "Design of a Hardware Accelerator for Multi-layer Maze Routing in VLSI and its Implementation on Virtex II Pro FPGA" in Proc. of IET UK Intl. Conf. on Information and Communication Technology in Electrical Sciences, ICTES 2007, at Dr. MGR University, Chennai, India, Dec 20-22, 2007, pp 817-821.
23. Kaleem Fatima, S. Vijay Gopal and N. Zeeshan Nadeem "A Novel Architecture for the Computation of 2D-DWT and its Implementation on Virtex-II Pro FPGA" in Proc. of International Conference on Computational Intelligence and Security, Harbin Institute of Technology, Harbin, China, pp: 531 - 535 Dec, 15 -19, 2007**. ISBN: 0-7695-3072-9**
24. Kaleem Fatima and Rameshwar Rao, "Design and Implementation of hardware Grid Routers on Virtex-II Pro FPGA," in Proc. of CITICOM 2007; International Conference

on Modeling and Simulation, Coimbatore Institute of Technology, Coimbatore, India, 27-29 Aug, 2007, pp 1099-1104.

IV. National Conference

1. Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Design and Implementation of Low Power Reversible Wallace Tree Multiplier using Compressors For High Speed Applications" at National Conference on Circuits, Signals and Systems during 22nd to 24th January, 2015 at Muffakam Jah College of Engineering and Technology, Hyderabad, India.ISBN:978-93-82570-47-9.
2. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi" Design and Implementation of Vedic Multiplier using Reversible Logic" at Third National Conference on Latest Trends in Signal Processing VLSI and Embedded Systems during June 2014, at Geethanjali College of Engineering and Technology, Hyd, India. ISBN978-93-83459-63-6, 2014,Bonfring
3. Nazeer Unnisa, Kaleem Fatima, and Md. Mahaboob Pasha, "A video coding scheme using Modified Joint Prediction Technique" in Proc. of NCECS 2011 – a national Conference on Emerging Trends in Communications and Signal Processing, pp 25 – Dept of ECE, ASCE College, 12th and 13th Oct-2011
4. Kaleem Fatima and Rameshwar Rao, "A Hardware Router for Multi-Terminal Nets with Efficient Rip-up and Reroute" in Proc. of NCVESCOM '08; National Conf on VLSI Embedded systems, Signals and Commns., Aarupadai Veedu Institute of Technology, Paiyanoor, TN, May, 8-9, 2008, pp 94-99.

V. Symposium

1. Dr. Kaleem Fatima and Mr. Rahmatullah Khan, "Implementation of Parallel Multilayer Wire Routing Machine for VLSI design, IETE Mid-Term Symposium, MTS-2013 on 21st - 22nd April, 2013, Hotel Green Park, Ameerpet, Hyderabad.